Design and Test of Field Programmable Gate Arrays in Space Applications

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Abstract - **Field Programmable Gate Arrays (FPGAUs) offer substantial benefits in terms of flexibility and design integration. In addition to qualifying this device for space applications by establishing its reliability and evaluating its sensitivity to radiation, screening the programmed devices with Automatic Test Equipment (ATE) and functional burn-in presents an interesting challenge. This paper presents a review of the design, qualification and screening cycle employed for FPGA designs in a space program, and demonstrates the need for close interaction between design and test engineers.**

1 FPGA Technology

Utilizing Actel Field Programmable Gate Arrays for flight designs has several advantages. The first is that the Actel FPGAUs are capable of being programmed with moderately complex designs. This eliminates the need for a great deal of 'glue logic' and can also take the place of complex logic that is not available in space qualified parts. The second is that the design cycle is much shorter than that of conventional gate arrays. This allows design changes in prototype hardware in as little as one hour instead of waiting eight weeks for a typical masked gate array. The last advantage is the ready availability of reliable, space qualified parts that only need be programmed and tested before use in a flight application.

2 Radiation Testing

However, a part is only acceptable for space applications if it can withstand the harshness of the applicable radiation environment. Of the FPGAUs available in 1990, only the 2000 gate Actel A1020, using antifuse technology, had demonstrated adequate radiation tolerance to make it a viable choice for space applications.

The Actel FPGAUs from the Matsushita foundry showed good radiation tolerance in all areas of concern. Total dose testing with Co-60 indicated that the Matsushita devices stay within data sheet parameters for doses above 100 Krads (Si), while those from the alternative Texas Instruments line perform poorly after only 6 Krads (Si). Examination of two versions of the Actel 1020 FPGA, the original 2.05 ACT1020-A from the Matsushita foundry and the 1.25 TI-1210D by Texas Instruments showed an acceptable amount of sensitivity to Single

Event Upsets for both parts. We will present a review of radiation testing by APL and others.

3 Device Qualification and Screening

Actel reports 37.4M device hours of dynamic burn-in on programmed devices at 125 deg C producing a failure rate of 83 FITS. We performed 1000 hour burn-in life test at 125 deg C on 8 sample programmed devices. No failures were observed. We will discuss the life test design.

4 Testing of Unprogrammed Devices

ActelUs functional screening of unprogrammed devices is quite comprehensive. Obtaining 883C qualified parts with Particle Impact Noise Detection (PIND) testing and additional 240 hour burn-in greatly simplified screening for APL. The major work then involved adequately screening the devices Rpost-programming.

5 Testing of Programmed Devices

Although the programmed devices represent Application Specific Integrated Circuits (ASICUs) of relatively low gate count, ensuring testability of the completed device is still important and complex. By following good Design for Testability (DFT) techniques the designer can enhance the testability of the device; thereby, significantly decreasing the cycle time for functional test development. Only then can a designer take true advantage of the short design turn-around time of FPGAUs.

Through cooperation between the design and test engineers, it is possible to develop simulation vectors appropriate for final electrical test. An in-house RCS program translated the simulation vectors from Mentor listings to the Sentry S-15 ATE tester environment. Ensuring the completeness of these vectors via fault-grading these vectors is still an area of concern. We will discuss these issues.

6 Screening of Programmed Devices

In order to successfully screen a completed FPGA for possible internal defects, it is necessary to combine a thorough electrical test program with a complete burn-in regimen. Each design required an individual set of burn-in circuitry, designed in-house. A discussion of this work is included.

7 Final Results

We will present a summary of the successes, as well as the failures and problems encountered for each of eight design types.